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| EXAMINER | |
|---|---|
| ZHE, MENG YAO | |
| **ART UNIT** | **PAPER NUMBER** |
| 2195 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/718,293 | BLAINEY ET AL. | |
| | Examiner | Art Unit | |
| | MengYao Zhe | 2195 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/20/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-31 are presented for examination.

### *Claim Rejections - 35 USC § 101*

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 14-21 recites a "system"; however, it appears that the system would reasonably be interpreted by one of ordinary skill in the art as software, per se, failing to be tangibly embodied or include any recited hardware as part of the apparatus.

### *Claim Rejections - 35 USC § 112*

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A. The following claim languages are unclear and indefinite:

i) Claim 1, it is uncertain what the relationship is between "a concurrently running process" of line 4 and "a concurrently running process" of line 8 <ie. Are they the same process? Does each process have two different array elements associated with it?>

Claims 14, 28, 30 have the same deficiencies as claim 1 above.

ii) Claim 24, lines 10-11, it is unclear as to what is meant by "check ...for said switch to said release state until detecting said release state" <i.e. if it has already detected a release state, why would it be checking for release state?>

Claim 25 has the same deficiencies as claim 24 above.

iii) Claims 1, 14, 24, 25, 26, 28, 30, it is unclear how the steps in these claims result in synchronization of the concurrently running processes <i.e. how does using two arrays and monitoring switching states result in synchronization?>

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 2, 6-14, 18-21, 23-31, are rejected under 35 U.S.C. 102(b) as being anticipated by Ishihata et al., Patent No. 5,278,975 (hereafter Ishihata).

8. As per claims 1, 14, 24, 25, 26, 28, 30, Ishihata teaches a method of synchronizing at least two concurrently running processes in a data processing system, comprising:

(a) providing a first array of elements with initialized states, each element of said first array having a concurrently running process associated therewith, each element of said first array being configured to have its state updated by its associated concurrently running process upon completion of a phase by said associated concurrently running process (Column 4, lines 50-58: the synchronization request register for each PE corresponds to an element of the array. The register is updated by the PE individually when it has decided to request for synchronization.);

(b) providing a second array of elements with initialized hold states, each element of said second array having a concurrently running process associated therewith, each element of said second array being configured to switch, upon receiving an instruction, to a release state (Column 4, lines 63-66; Column 10, lines 39-49: the status detecting register for each PE corresponds to each element of the second array; upon notification from the PEs that all is normal and synchronization detecting register

has detected that all synchronization request registers, which corresponds to the first array, are all logics of 1s, the status detection register, which corresponds to the second array changes to a different state, which is the release state.);

(c) arranging for monitoring said first array of elements and, upon each element of said first array having had its state updated, arranging for generating said instruction for switching said elements of said second array to said release state (Column 4, lines 63-66; Column 9, 58-Column 10, lines 12; The status detection register, which is the second array, turns into a release state, when the synchronization request register, which is the first array, sends out a signal that all array elements are 1s.).

9. As per claims 2, 29, 31, Ishihata teaches (d) for each process of said at least two concurrently running processes, configuring said each process such that, upon completion of said phase and upon updating of its associated element of said first array, said each process then waits at its associated element of said second array for said release state (Column 10, lines 20-25).

10. As per claim 6, Ishihata teaches upon said each element of said first array having had its state updated, and prior to generating said instruction for switching said elements of said second array to said release state, arranging for reinitializing each element of said first array (Column 10, lines 40-48).

11. As per claim 7, Ishihata teaches wherein in (c), said monitoring of said first array of elements is performed by one of said concurrently running processes (Column 10, lines 50-65).

12. As per claim 8, Ishihata teaches wherein in (c), said monitoring of said first array of elements is performed by an independent process (Column 10, lines 49-54).

13. As per claim 9, Ishihata teaches wherein in (a), said initialized state of said each element of said first array is a value (Column 4, lines 56-58).

14. As per claims 10, 18, Ishihata teaches wherein in (a), said each element of said first array comprises a state machine (Column 4, lines 56-58; Fig 15).

15. As per claims 11, 19, Ishihata teaches wherein said state machine is one of a counter, a gate, a flag and a sensor (Fig 15).

16. As per claims 12, 20, Ishihata teaches wherein in (b), said each element of said second array comprises a state machine (Fig 15).

17. As per claims 13, 21, Ishihata teaches wherein said state machine is one of a counter, a gate, a flag and a sensor (Fig 15).

18. As per claim 23, Ishihata teaches wherein said at least two concurrently running processes execute on multiple processors distributed across multiple computers connect across a network (Column 1, lines 7-15).

19. As per claim 27, Ishihata teaches wherein said process executed thereon is one of said concurrent processes (Column 2, lines 62-68).

### *Claim Rejections - 35 USC § 103*

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 3-5, 15-17, 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishihata et al., Patent No. 5,278,975 (hereafter Ishihata).

22. As per claim 3, 4, 15, 16, Ishihata does not specifically teach wherein each element of said first array has a byte size corresponding to the size of a cache line used in said data processing system. However, it would have been obvious to one having ordinary skill in the art at the time of the applicant's invention to allocate any size for the array as he wishes, including the size of a cache line, so that all data in the array may also fit in the cache line for quicker access.

23. As per claims 5, 17, Ishihata does not specifically teach providing each element of said second array locally in relation to its respective, associated process. However, it would have been obvious to one having ordinary skill in the art at the time of the applicant's invention to have all the element stored locally to its associated process for easier management and access.

24. As per claim 22, Ishihata does not specifically teach wherein said at least two concurrently running processes execute on multiple processors embodied within a single computer. However, it would have been obvious to one having ordinary skill in the art at the time of the applicant's invention to have multiple processes executing on

multiple processors within a single computer since multi-core processors are available at the time of the invention.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MengYao Zhe whose telephone number is 571-272-6946. The examiner can normally be reached on Monday Through Friday, 7:30 - 5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LEWIS A. BULLOCK, JR.
PRIMARY EXAMINER